

MEMORY

Buffered

4 M × 72 BIT SYNCHRONOUS DYNAMIC RAM DIMM

MB8504S072AC-100/-84/-67

200-pin, 2-bank, based on 2 M × 8 BIT SDRAMs with PLL

■ DESCRIPTION

The Fujitsu MB8504S072AC is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) module consisting of eighteen MB81117822A devices which organized as two banks of 1 M × 8 bits. This module is possible to minimize the skews of input signals such as clock and address signal by the PLL clock driver and register buffers mounted. The MB8504S072AC is optimized for those applications requiring high speed, high performance and large memory storage, and high density memory organizations.

This module is ideally suited for supercomputers, workstations, high-end PCs, laser printers, high resolution graphic adapters, accelerators, and other applications where a simple interface is needed.

■ PRODUCT LINE & FEATURES

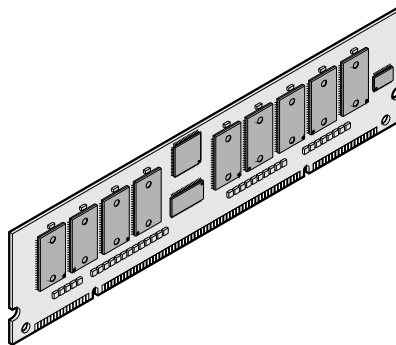
Parameter		MB8504S072AC-100	MB8504S072AC-84	MB8504S072AC-67
Clock Frequency		100 MHz max.	84 MHz max.	67 MHz max.
Burst Mode Cycle Time		10 ns max. (CL = 4) 15 ns max. (CL = 3)	12 ns max. (CL = 4) 17 ns max. (CL = 3)	15 ns max. (CL = 4) 20 ns max. (CL = 3)
RAS Access Time		54.5 ns max.	56.5 ns max.	60.5 ns max.
CAS Access Time		24.5 ns max.	26.5 ns max.	30.5 ns max.
Output Valid from Clock		9 ns max. (CL = 4) 9.5 ns max. (CL = 3)	9 ns max. (CL = 4) 9.5 ns max. (CL = 3)	9.5 ns max. (CL = 4) 10.5 ns max. (CL = 3)
Power Dissipation	Burst Mode	6253 mW max.	5782 mW max.	5314 mW max.
	Power Down Mode	572 mW max.	508 mW max.	443 mW max.

- Buffered 200-pin DIMM Socket Type (Lead pitch: 1.27 mm)
- Conformed to JEDEC Standard
- Organization: 4,194,304 words × 72 bits (ECC)
- Memory: MB81117822A (2 M × 8, 2-bank) × 18 pcs.
- 3.3 V ±0.3 V Supply Voltage
- All input/output LVTTTL compatible
- 2048 Refresh Cycle every 32.8 ms
- Auto and Self Refresh
- CKE Power Down Mode
- Output Enable and Input Data Mask
- PLL Clock Driver/Register Buffer/Input Buffer
- Module size: 1.5" (height) × 6.05" (length) × 0.16" (thick)

MB8504S072AC-100/-84/-67

■ PACKAGE

Plastic DIMM Package



(MDS-200P-P07)

Package and Ordering Information

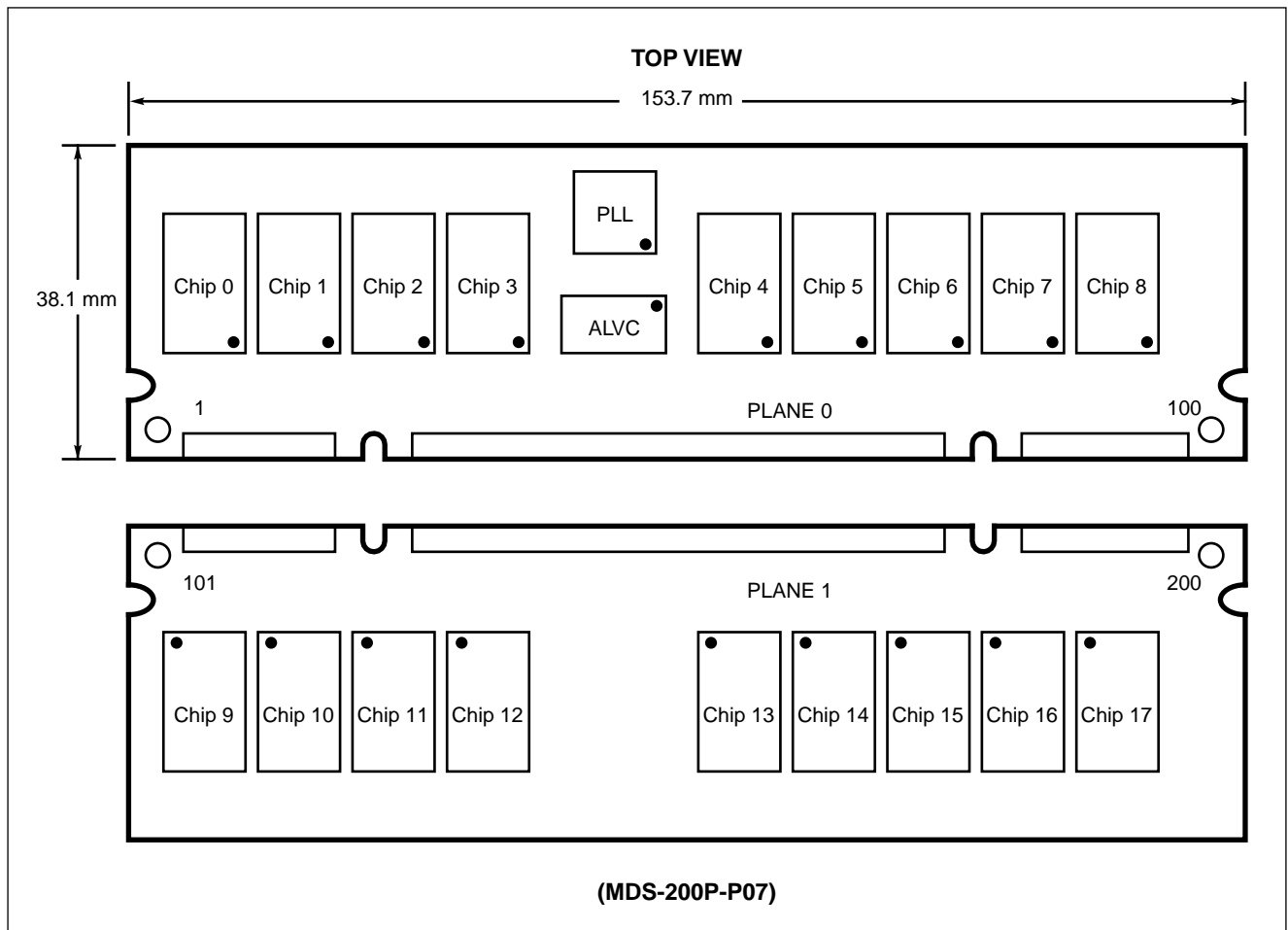
– 200-pad DIMM, order as MB8504S072AC-xxDG (DG = Gold Pad)

MB8504S072AC-100/-84/-67

■ PIN ASSIGNMENTS

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V _{CC}	41	V _{SS}	81	DQ ₁₅	121	DQ ₅₆	161	V _{SS}
2	N.C.	42	A ₈	82	DQ ₁₄	122	V _{CC}	162	DQ ₃₁
3	N.C.	43	A ₉	83	V _{SS}	123	DQ ₅₅	163	DQ ₃₀
4	IN	44	V _{CC}	84	DQ ₁₃	124	DQ ₅₄	164	V _{CC}
5	OUT	45	CKE ₁	85	DQ ₁₂	125	V _{SS}	165	DQ ₂₉
6	ID ₀	46	CKE ₀	86	V _{CC}	126	DQ ₅₃	166	DQ ₂₈
7	ID ₁	47	V _{SS}	87	DQ ₇	127	DQ ₅₂	167	V _{SS}
8	V _{SS}	48	$\overline{\text{CAS}}$	88	DQ ₆	128	V _{CC}	168	DQ ₂₃
9	DQ ₆₇	49	N.C.	89	V _{SS}	129	DQ ₄₇	169	DQ ₂₂
10	DQ ₆₆	50	V _{CC}	90	DQ ₅	130	DQ ₄₆	170	V _{CC}
11	V _{CC}	51	V _{SS}	91	DQ ₄	131	V _{SS}	171	DQ ₂₁
12	DQ ₆₅	52	$\overline{\text{RAS}}$	92	V _{CC}	132	DQ ₄₅	172	DQ ₂₀
13	DQ ₆₄	53	V _{SS}	93	$\overline{\text{PDE}}$	133	DQ ₄₄	173	V _{SS}
14	V _{SS}	54	N.C.	94	PD ₁	134	V _{CC}	174	N.C.
15	DQ ₆₃	55	N.C.	95	PD ₂	135	DQ ₃₉	175	N.C.
16	DQ ₆₂	56	V _{CC}	96	PD ₃	136	DQ ₃₈	176	V _{CC}
17	N.C.	57	A ₀	97	PD ₄	137	V _{SS}	177	N.C.
18	DQ ₆₁	58	A ₁	98	N.C.	138	DQ ₃₇	178	V _{SS}
19	DQ ₆₀	59	V _{SS}	99	N.C.	139	DQ ₃₆	179	V _{SS}
20	V _{CC}	60	DQ ₃₅	100	V _{SS}	140	V _{CC}	180	N.C.
21	N.C.	61	DQ ₃₄	101	N.C.	141	A ₆	181	N.C.
22	N.C.	62	V _{CC}	102	N.C.	142	A ₇	182	V _{CC}
23	V _{SS}	63	DQ ₃₃	103	V _{SS}	143	V _{SS}	183	DQ ₁₁
24	N.C.	64	DQ ₃₂	104	N.C.	144	A ₁₁	184	DQ ₁₀
25	N.C.	65	V _{SS}	105	N.C.	145	N.C.	185	V _{SS}
26	V _{CC}	66	DQ ₂₇	106	N.C.	146	V _{CC}	186	DQ ₉
27	DQ ₅₁	67	DQ ₂₆	107	ID ₂	147	DQM	187	DQ ₈
28	DQ ₅₀	68	V _{CC}	108	DQ ₇₁	148	$\overline{\text{WE}}$	188	V _{CC}
29	V _{SS}	69	DQ ₂₅	109	DQ ₇₀	149	V _{SS}	189	DQ ₃
30	DQ ₄₉	70	DQ ₂₄	110	V _{SS}	150	N.C.	190	DQ ₂
31	DQ ₄₈	71	V _{SS}	111	DQ ₆₉	151	CLK	191	V _{SS}
32	V _{CC}	72	DQ ₁₉	112	DQ ₆₈	152	V _{CC}	192	DQ ₁
33	DQ ₄₃	73	DQ ₁₈	113	V _{CC}	153	$\overline{\text{CS}}_1$	193	DQ ₀
34	DQ ₄₂	74	V _{CC}	114	N.C.	154	$\overline{\text{CS}}_0$	194	PD ₅
35	V _{SS}	75	DQ ₁₇	115	V _{SS}	155	V _{SS}	195	PD ₆
36	DQ ₄₁	76	DQ ₁₆	116	N.C.	156	N.C.	196	PD ₇
37	DQ ₄₀	77	V _{SS}	117	DQ ₅₉	157	A ₁₀	197	PD ₈
38	V _{CC}	78	N.C.	118	DQ ₅₈	158	V _{CC}	198	V _{CC}
39	A ₄	79	N.C.	119	V _{SS}	159	A ₂	199	N.C.
40	A ₅	80	V _{CC}	120	DQ ₅₇	160	A ₃	200	N.C.

MB8504S072AC-100/-84/-67



■ PIN DESCRIPTION

Symbol	I/O	Function	Symbol	I/O	Function
A ₀ to A ₁₁	I	Address Input	DQ ₀ to DQ ₇₁	I/O	Data Input/Data Output
RAS	I	Row Address Strobe	V _{CC}	—	Power Supply (+3.3 V)
CAS	I	Column Address Strobe	V _{SS}	—	Ground (0 V)
WE	I	Write Enable	N.C.	—	No Connection
DQM	I	Data (DQ) Mask	PD ₁ to PD ₈	O	Presence Detect
CLK	I	Clock Input	ID ₀ to ID ₂	O	ID bit
CKE ₀ , CKE ₁	I	Clock Enable	PDE	I	Presence Detect Enable
CS ₀ , CS ₁	I	Chip Select			

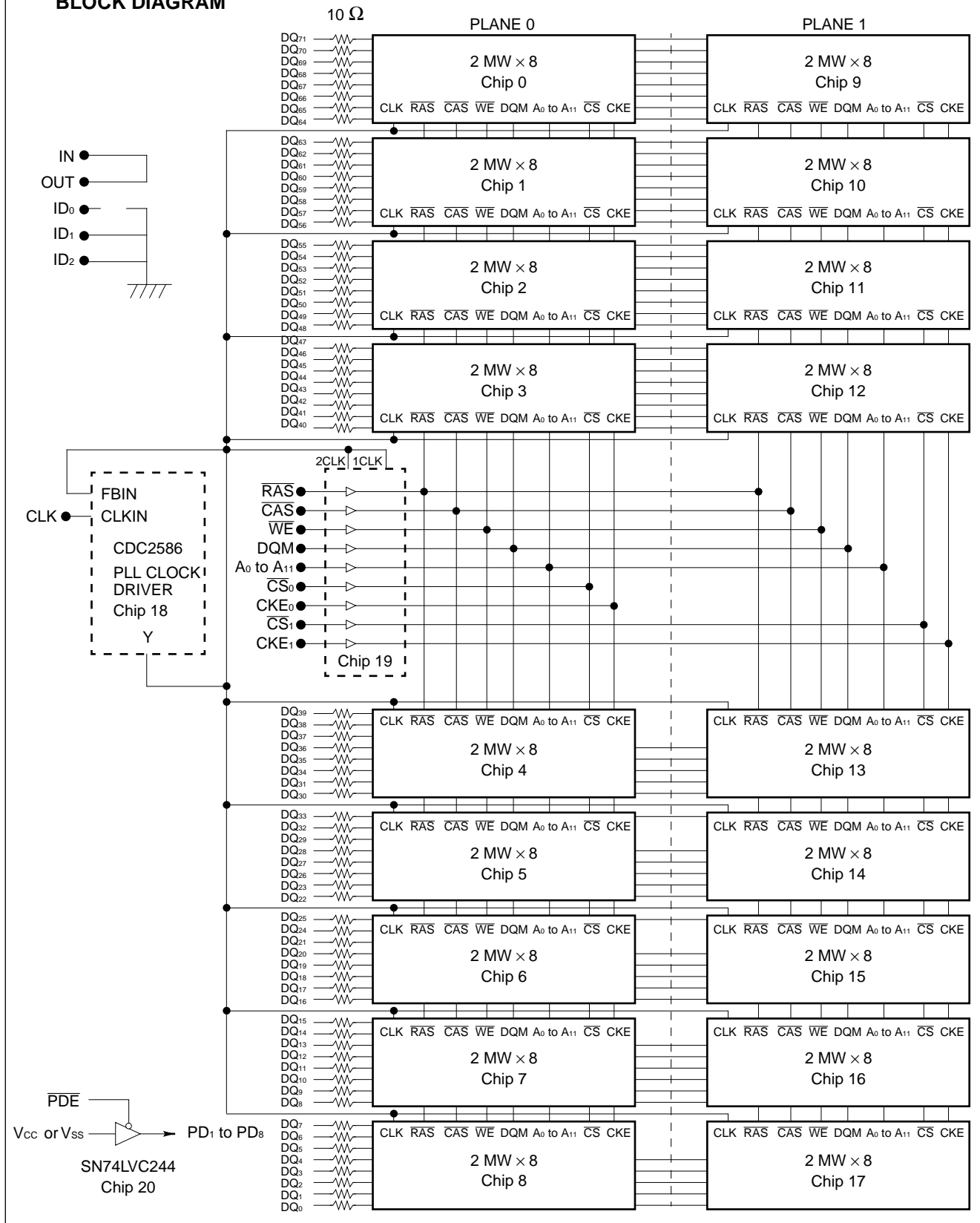
MB8504S072AC-100/-84/-67

■ PRESENCE DETECT(PD)/ID DEFINITION

Symbol	MB8504S072AC -100	MB8504S072AC -84	MB8504S072AC -67	Description of PD/ID
PD ₁	H	H	H	MODULE CONFIGURATION, SDRAM ORGANIZATION, AND ADDRESSING; Module Configuration: 4 M × 72 Mounted SDRAM Configuration: 2 M × 8 SDRAM Address (Row/Column): 12/9
PD ₂	L	L	L	
PD ₃	L	L	L	
PD ₄	L	L	L	
PD ₅	H	L	H	MODULE SPEED; 10 ns: PD ₅ = H, PD ₆ = L 12 ns: PD ₅ = L, PD ₆ = H 15 ns: PD ₅ = H, PD ₆ = H
PD ₆	L	H	H	
PD ₇	H	H	H	BUFFERING; Buffered: PD ₇ = H
PD ₈	H	H	H	BYTE WRITE; Word: PD ₈ = H
ID ₀	OPEN	OPEN	OPEN	COLUMN TO COLUMN COMMAND INTERVAL; 1 Clock: ID ₀ = OPEN
ID ₁	V _{SS}	V _{SS}	V _{SS}	READ PRECHARGE POSITION; No Early RAS: ID ₁ = V _{SS}
ID ₂	V _{SS}	V _{SS}	V _{SS}	POWER; Normal: ID ₂ = V _{SS}

MB8504S072AC-100/-84/-67

BLOCK DIAGRAM



MB8504S072AC-100/-84/-67

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage*	V _{CC}	-0.5	+4.6	V
Input Voltage*	V _{IN}	-0.5	+4.6	V
Output Voltage*	V _{OUT}	-0.5	+4.6	V
Storage Temperature	T _{STG}	-55	+125	°C
Power Dissipation	P _D	—	12	W
Output Current (D.C.)	I _{OUT}	-50	+50	mA

* : Voltages referenced to V_{SS} (= 0 V)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	*1	V _{CC}	3.0	3.3	3.6	V
		V _{SS}	0	0	0	V
Input High Voltage, All Inputs	*1	V _{IH}	2.0	—	V _{CC} +0.5	V
Input Low Voltage, All Inputs	*1	V _{IL}	-0.5	—	0.8	V
Ambient Temperature		T _A	0	—	+70	°C

*1. Voltages referenced to V_{SS} (= 0 V)

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(V_{CC} = +3.3 V, f = 1 MHz, T_A = +25°C)

Parameter	Symbol	Value		Unit	
		Min.	Max.		
Input Capacitance	A ₀ to A ₁₁	C _{IN1}	—	10	pF
	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, WE	C _{IN2}	—	10	pF
	$\overline{\text{CS}}_0$, $\overline{\text{CS}}_1$	C _{IN3}	—	10	pF
	CKE ₀ , CKE ₁	C _{IN4}	—	10	pF
	CLK	C _{IN5}	—	10	pF
	DQM	C _{IN6}	—	10	pF
Input/Output Capacitance	DQ ₀ to DQ ₇₁	C _{DQ}	—	13	pF

MB8504S072AC-100/-84/-67

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	Condition	Value		Unit		
				Min.	Max.			
Operating Current (Average Power Supply Current)	*2	MB8504S072AC-100	No Burst; $t_{CK} = \text{min}$ $t_{RC} = \text{min}$ One Bank Active	—	1190	mA		
		MB8504S072AC-84		—	1120	mA		
		MB8504S072AC-67		—	1051	mA		
	MB8504S072AC-100	*2	MB8504S072AC-100	No Burst; $t_{CK} = \text{min}$ $t_{RC} = \text{min}$ All Banks Active	—	1640	mA	
					MB8504S072AC-84	—	1518	mA
					MB8504S072AC-67	—	1396	mA
Precharge Standby Current (Power Supply Current)	*2	MB8504S072AC-100	CKE = V_{IL} , $t_{CK} = \text{min}$ All Banks Idle	—	159	mA		
		MB8504S072AC-84		—	141	mA		
		MB8504S072AC-67		—	123	mA		
	MB8504S072AC-100	*2	MB8504S072AC-100	CKE = V_{IH} , $t_{CK} = \text{min}$ All Banks Idle	—	636	mA	
					MB8504S072AC-84	—	621	mA
					MB8504S072AC-67	—	607	mA
Active Standby Current (Power Supply Current)	*2	MB8504S072AC-100	CKE = V_{IL} , $t_{CK} = \text{min}$ Any Bank Active	—	636	mA		
		MB8504S072AC-84		—	621	mA		
		MB8504S072AC-67		—	607	mA		
	MB8504S072AC-100	*2	MB8504S072AC-100	CKE = V_{IH} , $t_{CK} = \text{min}$ Any Bank Active	—	816	mA	
					MB8504S072AC-84	—	801	mA
					MB8504S072AC-67	—	787	mA
Burst Mode Current (Average Power Supply Current)	*2	MB8504S072AC-100	$t_{CK} = \text{min}$	—	1737	mA		
		MB8504S072AC-84		—	1606	mA		
		MB8504S072AC-67		—	1476	mA		
Auto-refresh Current (Average Power Supply Current)	*2	MB8504S072AC-100	Auto Refresh $t_{CK} = \text{min}$ $t_{RC} = \text{min}$ $t_{RRD} = \text{min}$	—	1377	mA		
		MB8504S072AC-84		—	1269	mA		
		MB8504S072AC-67		—	1161	mA		
Self-refresh Current (Average Power Supply Current)	*2	MB8504S072AC-100	$t_{CK} = V_{IL}$	—	384	mA		
		MB8504S072AC-84		—	369	mA		
		MB8504S072AC-67		—	355	mA		
Input Leakage Current (All inputs except DQ)		$I_{I(L)}$	$V_{IN} = 0\text{ V}$	-10	10	μA		
			$V_{IN} = V_{CC}$	-10	10			
Input Hold Current (All inputs except CLK, $\overline{\text{PDE}}$, DQ)		$I_{I(\text{Hold})}$	$V_{IN} = 0.8\text{ V}$	75	—	μA		
			$V_{IN} = 2\text{ V}$	—	-75			
Output Leakage Current (All DQ)		$I_{O(L)}$	Output is disabled (Hi-Z) $0\text{ V} \leq V_{OUT} \leq V_{CC}$ $3.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	-10	10	μA		
LVTTL Output High Voltage	*1	V_{OH}	$I_{OH} = -2.0\text{ mA}$	2.4	—	V		
LVTTL Output Low Voltage	*1	V_{OL}	$I_{OL} = +2.0\text{ mA}$	—	0.4	V		

MB8504S072AC-100/-84/-67

- Notes:**
- *1. Voltages referenced to V_{SS} (= 0 V)
 - *2. I_{CC} depends on the output termination, load conditions, clock cycle rate and signal clock rate. The specified values are obtained with the output open and no termination register.
 - *3. An initial pause (DESL on NOP) of 200 μ s is required after power-on followed by a minimum of eight Auto-refresh cycles.
 - *4. Values except I_{CC2P} are for when one side of the double-sided module is in standby mode and the other side has two banks active in burst mode.

MB8504S072AC-100/-84/-67

■ AC CHARACTERISTICS

(1) BASE CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Notes	Symbol	MB8504S072AC -100		MB8504S072AC -84		MB8504S072AC -67		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Clock Period	CL = 4	t _{CK}	10	20	12	20	15	20	ns
		CL = 3		15	20	17	20	20	20	ns
2	Clock High Time		t _{CH}	4	—	4.8	—	6	—	ns
3	Clock Low Time		t _{CL}	4	—	4.8	—	6	—	ns
4	$\overline{\text{CS}}$ Set Up Time		t _{SC}	3.4	—	3.4	—	3.4	—	ns
5	$\overline{\text{CS}}$ Hold Time		t _{HC}	1	—	1	—	1	—	ns
6	Input Set Up Time		t _{SI}	3.4	—	3.4	—	3.4	—	ns
7	Input Hold Time		t _{HI}	1	—	1	—	1	—	ns
8	Data Input Set Up Time		t _{SID}	3.5	—	3.5	—	3.5	—	ns
9	Data Input Hold Time		t _{HID}	1.5	—	1.5	—	1.5	—	ns
10	Output Valid from Clock (t _{CLK} = min)	*1, *2 CL = 4	t _{AC}	—	9	—	9	—	9.5	ns
		CL = 3		—	9.5	—	9.5	—	10.5	
11	Output in Low-Z		t _{OLZ}	2.5	—	2.5	—	2.5	—	ns
12	Output in High-Z	*3	t _{OHZ}	2.5	—	2.5	—	2.5	—	ns
13	Output Hold Time		t _{OH}	2.5	—	2.5	—	2.5	—	ns
14	Time between Refresh		t _{REF}	—	32.8	—	32.8	—	32.8	ms
15	Transition Time		t _r	0.5	2	0.5	2	0.5	2	ns
16	Power Down Exit Time		t _{PDE}	3.5	—	4.5	—	5.5	—	ns

MB8504S072AC-100/-84/-67

(2) BASE VALUES FOR CLOCK COUNT/LATENCY

No.	Parameter	Notes	Symbol	MB8504S072AC -100		MB8504S072AC -84		MB8504S072AC -67		Unit
				Min.	Max.	Min.	Max.	Min..	Max.	
1	$\overline{\text{RAS}}$ Cycle Time	*4	t _{RC}	90	—	100	—	110	—	ns
2	$\overline{\text{RAS}}$ Access Time	*5	t _{RAC}	—	54.5	—	56.5	—	60.5	ns
3	$\overline{\text{CAS}}$ Access Time	*6, *9	t _{CAC}	—	24.5	—	26.5	—	30.5	ns
4	$\overline{\text{RAS}}$ Precharge Time		t _{RP}	30	—	35	—	40	—	ns
5	$\overline{\text{RAS}}$ Active Time		t _{RAS}	60	100000	65	100000	70	100000	ns
6	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*7	t _{RCD}	30	—	30	—	30	—	ns
7	Write Recovery Time		t _{WR}	10	—	12	—	15	—	ns
8	Write Precharge Time		t _{RWL}	10	—	12	—	15	—	ns
9	$\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ Bank Active Delay Time		t _{RRD}	30	—	30	—	30	—	ns

(3) CLOCK COUNT FORMULA (*8)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad (\text{Round off a whole number})$$

(4) LATENCY (The latency values on these parameters are fixed regardless of clock period.)

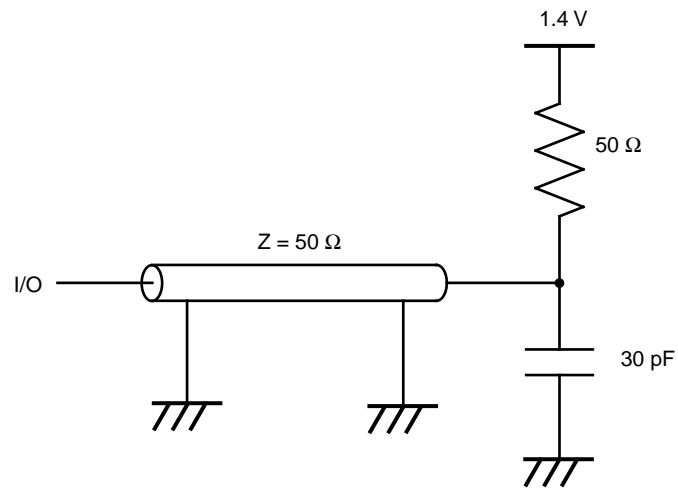
No.	Parameter	Symbol	MB8504S072AC -100	MB8504S072AC -84	MB8504S072AC -67	Unit
1	CKE to Clock Disable	t _{CKE}	2	2	2	Cycle
2	DQM to Output in High-Z	t _{DQZ}	3	3	3	Cycle
3	DQM to Input Data Delay	t _{DQD}	1	1	1	Cycle
4	Last Output to Write Command Delay	t _{OWD}	1	1	1	Cycle
5	Write Command to Input Data Delay	t _{DWD}	1	1	1	Cycle
6	Precharge to Output in High-Z Delay	CL = 4	4	4	4	Cycle
		CL = 3	3	3	3	Cycle
7	Mode Register Access to Bank Active (min)	t _{MRD}	2	2	2	Cycle
8	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay (min)	t _{CCD}	1	1	1	Cycle
9	$\overline{\text{CAS}}$ Bank Delay (min)	t _{CBD}	1	1	1	Cycle

MB8504S072AC-100/-84/-67

- Notes:**
- *1. Assumes t_{RCD} and t_{CAC} are satisfied.
 - *2. t_{AC} also specifies the access time at burst mode except for first access.
 - *3. Specified where output buffer is no longer driven.
 - *4. Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}).
 - *5. t_{RAC} is a reference value. Maximum value is obtained from the sum of t_{RCD} (min) and t_{CAC} (max).
 - *6. Assumes t_{RAC} and t_{AC} are satisfied.
 - *7. Operation within the t_{RCD} (min) ensures that t_{RAC} can be met; if t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{CAC} and t_{AC} .
 - *8. All base values are measured from the clock edge at the command input to the clock edge for the next command input.
All clock counts are calculated by a simple formula:
clock count equals base value divided by clock period (round off to a whole number).
 - *9. The I_{CAC} (\overline{CAS} latency: CL) is programmed by the mode register.
 - *10. An initial pause (\overline{DESL} on NOP) of 200 μs is required after power-up followed by a minimum of eight Auto-refresh cycles.
 - *11. 1.4 V or V_{REF} is the reference level for measuring timing of signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max).
 - *12. AC characteristics assume $t_T = 1$ ns and 30 pF of capacitive load.
- *Source: See MB81117822A Data Sheet for details on the electricals.

MB8504S072AC-100/-84/-67

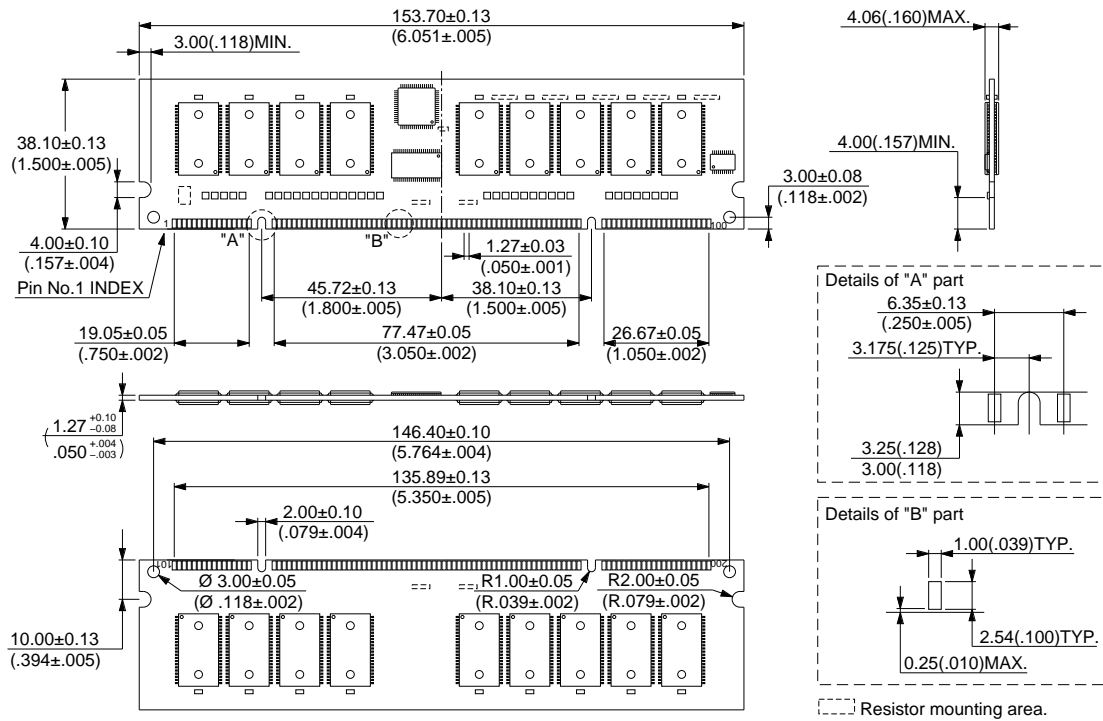
■ AC OPERATING TEST CONDITION (Example of AC Test Load Circuit)



MB8504S072AC-100/-84/-67

■ PACKAGE DIMENSION

200-PAD PLASTIC DUAL IN-LINE TYPE MODULE (CASE No.: MDS-200P-P07)



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